JEDEC STANDARD

Ball Grid Array Pinout for 1-, 2-, and 3-Bit Logic Functions

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BALL GRID ARRAY PINOUTS STANDARDIZED FOR 1-, 2-, AND 3-BIT LOGIC FUNCTIONS

(Formerly JEDEC Board Ballot JCB-03-65, formulated under the cognizance of the JC-40 Committee on Digital Logic.)

1 Scope

This standard defines device pinout for 1-, 2- and 3-bit wide logic functions. This pinout specifically applies to the conversion of Dual-Inline-Packaged (DIP) 1-, 2- and 3-bit logic devices to DSBGA-packaged 1-, 2- and 3-bit logic devices.

The purpose of this document is to provide a pinout standard for 1-, 2- and 3-bit logic devices offered in 5-, 6- or 8-ball Die-Sized Ball Grid Array (DSBGA) packages for uniformity, multiplicity of sources, elimination of confusion, ease of device specification, and ease of use.

2 Terms and definitions (for the purpose of this document)

DIP: Dual In-line Pin Package (gull-wing)

SSOP: Shrink Small-Outline Package; 0.65-mm lead pitch; 5.3-mm wide body (MO-150)

TSSOP: Thin Shrink Small-Outline Package; 0.65-mm lead pitch; 4.4-mm wide body (MO-153)

TVSOP: Thin Very Small-Outline Package; 0.4-mm lead pitch; 4.4-mm wide body (MO-194)

DSBGA:Die-Sized Ball Grid Array; 0.5-mm ball pitch (MO-211)

3 Pinout standard

3.1 Description

The following criteria shall be used to convert existing 1-, 2- and 3-bit logic device functions offered in 5-, 6- and 8-pin DIP packages (e.g. SSOP, TSSOP, TVSOP) to 1-, 2- and 3-bit logic device functions offered in the 5-, 6- and 8-ball DSBGA packages:

A. Attributes for the DSBGA package area as indicated below:

5-Ball, 0.50-mm ball pitch with 0.90-mm × 1.40-mm body size and 3-row × 2-column ball matrix, depopulated from 6-ball, MO-211, Variation EA.

6-Ball, 0.50-mm ball pitch with 0.90-mm × 1.40-mm body size and 3-row × 2-column ball matrix, MO-211, Variation EA.

8-Ball, 0.50-mm ball pitch with 0.90-mm × 1.90-mm body size and 4-row × 2-column ball matrix, MO-211, Variation EA.

B. The pinout conversions shall be in accordance with the diagrams shown in sections 3.2, 3.4 and 3.6. Each device shall be pinned out based on its present package/pinout and the pinout tables in sections 3.3, 3.5, and 3.7.

3.2 5-ball DSBGA (MO-211)

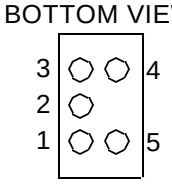

Figure 1 — Pinout configuration

3 Pinout standard (cont'd)

3.3 Pin conversion from 5-pin DIP to 5-ball DSBGA

The pinout adopts the naming convention of logic devices in 5-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 1 — 5-pin pinout table

Function (See Note)	Description	Pin Numbers				
		1	2	3	4	5
1G00	Single 2-input NAND gate	A	B	GND	Y	V_{DD}
1G02	Single 2-input NOR gate	A	B	GND	Y	V_{DD}
1G04	Single inverter	DNU	A	GND	Y	V_{DD}
1GU04	Single unbuffered inverter	DNU	A	GND	Y	V_{DD}
1G05	Inverter with open-drain output	DNU	A	GND	Y	V_{DD}
1G06	Inverter with open-drain output	DNU	A	GND	Y	V_{DD}
1G07	Single buffer/driver with open-drain output	DNU	A	GND	Y	V_{DD}
1G08	Single 2-input AND gate	A	B	GND	Y	V_{DD}
1G14	Single inverter with Schmitt-trigger input	DNU	A	GND	Y	V_{DD}
1G17	Single buffer/driver with Schmitt-trigger input	DNU	A	GND	Y	V_{DD}
1G32	Single 2-input OR gate	A	B	GND	Y	V_{DD}
1G34	Single buffer	DNU	A	GND	Y	V_{DD}
1G38	Single 2-input NAND gate with open-drain output	A	B	GND	Y	V_{DD}
1G66	Single analog switch	I/O	I/O	GND	OE	V_{DD}
1G79	D-type flip-flop with Q output	D	CK	GND	Q	V_{DD}
1G80	D-type flip-flop with $\overline{Q}$ output	D	CK	GND	$\overline{Q}$	V_{DD}
1G86	Single 2-input XOR gate	A	B	GND	Y	V_{DD}
1G125	Single buffer/driver with 3-state outputs	$\overline{OE}$	A	GND	Y	V_{DD}
1G125	Single bus switch	$\overline{OE}$	A	GND	B	V_{DD}
1G126	Single buffer/driver with 3-state outputs	OE	A	GND	Y	V_{DD}
1G240	Single inverter with 3-state outputs	$\overline{OE}$	A	GND	Y	V_{DD}
1G384	Single bus switch	A	B	GND	$\overline{OE}$	V_{DD}

NOTE 1 The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer-specific characters to make up a complete part designation.

NOTE 2 DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

NOTE

3.4 6-ball DSBGA (MO-211)

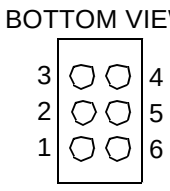

Figure 2 — Pinout configuration

3 Pinout standard (cont'd)

3.5 Pin conversion from 6-pin DIP to 6-ball DSBGA

The pinout adopts the naming convention of logic devices in 6-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 2 — 6-pin pinout table

Function	Description	Pin Numbers					
		1	2	3	4	5	6
2G04	Dual inverter	1A	GND	2A	2Y	V_{DD}	1Y
2GU04	Dual unbuffered inverter	1A	GND	2A	2Y	V_{DD}	1Y
2G06	Dual inverter with open-drain outputs	1A	GND	2A	2Y	V_{DD}	1Y
2G07	Dual buffer/driver with open-drain outputs	1A	GND	2A	2Y	V_{DD}	1Y
1G10	Single 3-input NAND gate	A	GND	B	Y	V_{DD}	C
1G11	Single 3-input AND gate	A	GND	B	Y	V_{DD}	C
2G14	Dual inverter with Schmitt-trigger inputs	1A	GND	2A	2Y	V_{DD}	1Y
2G16	Dual buffer	1A	GND	2A	2Y	V_{DD}	1Y
2G17	Dual buffer/driver with Schmitt-trigger inputs	1A	GND	2A	2Y	V_{DD}	1Y
1G18	1-of-2 non-inverting demux with 3-state output	S	GND	A	1Y	V_{DD}	0Y
1G19	1-of-2 decoder/multiplexer	A	GND	$\overline{OE}$	1Y	V_{DD}	0Y
1G27	Single 3-input NOR	A	GND	B	Y	V_{DD}	C
2G34	Dual buffer/driver	1A	GND	2A	2Y	V_{DD}	1Y
1G57	Universal configurable 2-input gate	In1	GND	In0	Y	V_{DD}	In2
1G58	Universal configurable 2-input gate	In1	GND	In0	Y	V_{DD}	In2
1G97	Universal configurable 2-input gate	In1	GND	In0	Y	V_{DD}	In2
1G98	Universal configurable 2-input gate	In1	GND	In0	Y	V_{DD}	In2
1G157	Single 2-input non-inverting multiplexer	In1	GND	In0	Y	V_{DD}	S
1G158	Single 2-input inverting multiplexer	In1	GND	In0	$\overline{Y}$	V_{DD}	S
1G175	Single D-type flip-flop	CK	GND	D	Q	V_{DD}	CLR
1G332	Single 3-input OR	A	GND	B	Y	V_{DD}	C
1G386	Single 3-input XOR	A	GND	B	Y	V_{DD}	C
1G373	Single D-type latch	LE	GND	D	Q	V_{DD}	$\overline{OE}$
1G374	Single D-type flip-flop	CK	GND	D	Q	V_{DD}	$\overline{OE}$
1G3157	SPDT analog switch	I/O2	GND	I/O1	COM	V_{DD}	S
1G3257	2-to-1 bus-switch multiplexer	B2	GND	B1	A	V_{DD}	S

NOTE 1 The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer-specific characters to make up a complete part designation.

NOTE 2 DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

3 Pinout standard (cont'd)

3.6 8-ball DSBGA (MO-211)

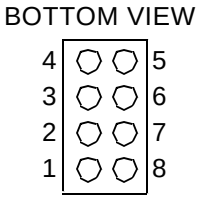

Figure 3 — Pinout configuration

3.7 Pin conversion from 8-pin DIP to 8-ball DSBGA

The pinout adopts the naming convention of logic devices in 8-pin DIP packages. The signal nomenclature used in this table is intended to define the functionality of each pin and not require that a specific naming convention be followed. Each product vendor is free to name the pin according to their own conventions, provided that the functionality of the device is not altered from what is specified here.

Table 3 — 8-pin pinout table

Function	Description	Pin Numbers							
		1	2	3	4	5	6	7	8
2G00	Dual 2-input NAND gate	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G02	Dual 2-input NOR gate	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G08	Dual 2-input AND gate	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G32	Dual 2-input OR gate	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G38	Dual 2-input NAND gate with open-drain output	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G53	Dual analog MUX/DEMUX	COM	INH	GND	GND	S	I/O2	I/O1	V_{DD}
2G66	Dual analog switch	1I/O	1I/O	2OE	GND	2I/O	2I/O	1OE	V_{DD}
2G74	Single D-type flip-flop	CK	D	$\overline{Q}$	GND	Q	$\overline{CLR}$	$\overline{PRE}$	V_{DD}
2G79	Dual D-type flip-flop	1CK	1D	2Q	GND	2CK	2D	1Q	V_{DD}
2G80	Dual D-type flip-flop with inverting Q outputs	1CK	1D	$2\overline{Q}$	GND	2CK	2D	$1\overline{Q}$	V_{DD}
2G86	Dual 2-input XOR gate	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G125	Dual buffer/driver with 3-state outputs	$1\overline{OE}$	1A	2Y	GND	2A	1Y	$2\overline{OE}$	V_{DD}
2G126	Dual buffer/driver with 3-state outputs	1OE	1A	2Y	GND	2A	1Y	2OE	V_{DD}
2G132	Dual 2-input NAND gate with schmitt-trigger inputs	1A	1B	2Y	GND	2A	2B	1Y	V_{DD}
2G139	Single 2-to-4 decoder	A	B	Y4	GND	Y3	Y2	Y1	V_{DD}
2G157	Single MUX/DEMUX	A	B	$\overline{Y}$	GND	Y	S	$\overline{G}$	V_{DD}
2G240	Dual inverting buffer with 3-state outputs	$1\overline{OE}$	1A	2Y	GND	2A	1Y	$2\overline{OE}$	V_{DD}
2G241	Dual buffer/driver with 3-state outputs	$1\overline{OE}$	1A	2Y	GND	2A	1Y	2OE	V_{DD}

Table 3 — 8-pin pinout table

Function	Description	Pin Numbers							
		1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
2G244	Dual buffer/driver with 3-state outputs	$1\overline{OE}$	1A	2Y	GND	2A	1Y	$2\overline{OE}$	V_{DD}
3G04	Triple inverter	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3GU04	Triple unbuffered inverter	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G05	Triple inverter with open-drain outputs	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G06	Triple inverter with open-drain outputs	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G07	Triple buffer/driver with open-drain outputs	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G14	Triple inverter with Schmitt-trigger inputs	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G17	Triple buffer/driver with Schmitt-trigger inputs	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}
3G34	Triple buffer/driver	1A	3Y	2A	GND	2Y	3A	1Y	V_{DD}

NOTE 1 The function designation refers to the part designation of a series of commercial logic parts common in the industry. This number is normally preceded by a series of manufacturer-specific characters to make up a complete part designation.

NOTE 2 DNU means Do Not Use. This designation requires that the printed circuit landing-pad for this device terminal remain unconnected to any signal or supply potential. It must remain an open circuit. This device terminal might be connected to active or inactive circuitry within the device.

4 Reference to other applicable JEDEC standards and publications

JEP95, *JEDEC Registered and Standard Outlines for Solid State and Related Product*

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